

REMARKS

This is in full and timely response to the above-identified Office Action. The above listing of the claims supersedes any previous listing. Favorable reexamination and reconsideration are respectfully requested in view of the preceding amendments and the following remarks.

Claim Status

Claims 7-15 are pending in the application. Claims 7-10 and 14 stand rejected as being anticipated by Fang (US 6,667,511). Claims 11-13 and 15 stand rejected as being unpatentable over Fang (US 6,667,511) in view of Sheng et al. (US 5,981,404). Reconsideration and allowance of the present application based on the following remarks is carefully requested.

Claim Amendments

Applicant has amended claims 7 and 13 to clarify the subject matter for which protection is sought.

Rejections under 35 U.S.C. § 102

The rejection of claims 7-10 and 14 under 35 U.S.C. § 102(e) as being anticipated by Fang (US 6,667,511) is respectfully traversed.

This rejection relies on Figs. 5g and 5l of Fang as a basis of the anticipation. However, a careful review reveals that these figures do not in fact provide disclosure that anticipates the claimed subject matter. The cited figures show a device isolation structure, a tunnel oxide layer, a floating gate, a dielectric layer and a control gate layer are formed over a semiconductor substrate in a cell region and the device isolation structure.

However, the dielectric layer is not formed over the semiconductor substrate in a peripheral circuit region.

The claimed arrangement, on the other hand, calls for the dielectric layer to be formed over the floating gate layer in the cell region and over the semiconductor substrate in the peripheral region. The dielectric layer which is formed over both the

cell and peripheral regions includes an oxide layer and a nitride layer (e.g. an ONO layer).

Fig. 5l of Fang discloses a gate oxide 152 and a poly 2 gate region 154 in a low voltage peripheral transistor 150 and a gate oxide 162 and a poly 2 gate 164 in a high voltage peripheral transistor 160. Claim 7 calls for a dielectric layer including an oxide layer and a nitride layer to be provided in both the cell and peripheral regions. Fig. 5l of Fang, however, merely discloses gate oxide 152 and 162 and fails to disclose/suggest the use of an ONO layer in this peripheral location.

The rejection also relies on Figs. 7a and 7b of Fang. A careful study of these figures reveals that Fang merely disclose a stacked gate flash memory cell in a core region 7a and a select gate transistor in the core region 7b, but does not teach or disclose an ONO dielectric being formed over a peripheral circuit region.

For at least these reasons, the Applicant respectfully submits that claim 7 is not anticipated by Fang. Claims 8-10 and 14 which are dependent on claim 7 are therefore allowable for the reasons discussed above with respect to claim 7, as well as on their individual merit.

#### Rejections under 35 U.S.C. § 103

The rejections of claims 11-13 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Fang (US 6,667,511) in view of Sheng et al. (US 5,981,404), are respectively traversed.

Claims 11-12, which are dependent upon claim 7, are patentable for at least the reasons discussed above in connection with 7, as well as on their individual merits.

In connection with claims 13 and 15, the Examiner relies on Figs. 5g, 5l, 7a and 7b of Fang, and Figs. 6 and 9 of Sheng. A careful review of these figures reveals that Fang merely discloses a stacked gate flash memory cell in a core region 7a, and a select gate transistor in the core region 7b, but does not (as noted *supra*) teach or suggest that an ONONO dielectric is formed over a peripheral circuit region.

In contradistinction, claim 13 calls for the dielectric layer which includes a first

oxide layer, a first nitride layer, a second oxide layer, a second nitride layer and a third oxide layer, to be formed over the semiconductor substrate in the peripheral region. Neither Fang nor Sheng teach or disclose such a structure.

Indeed, all that Sheng can be relied upon is to teach a conventional method of forming the dielectric layer referred to as column 10, lines 36-38 of Fang, and contains nothing that would lead the hypothetical person of ordinary skill to consider a modification of the basic arrangement disclosed in Fang.

That is to say, in order to establish a *prima facie* case of obviousness, it is necessary to show that the hypothetical person of ordinary skill would, without any knowledge of the claimed subject matter and without any inventive activity, be motivated to arrive at the claimed subject matter given the guidance of the cited references when each is fully considered as statutorily required. Note also needs to be taken that the person of ordinary skill in the art "thinks along the lines of conventional wisdom in the art and is not one who undertakes to innovate *Standard Oil Co. v American Cyanamid Co.*, 227 USPQ2d 293, 298 (Fed. Cir. 1985).

It is submitted that "innovation" would be necessary in order to take the teachings of Fang and arrive at the claimed subject matter.

Accordingly, Applicant respectfully submits that claim 13 is not rendered unpatentable in light of the teachings of either Fang or Sheng taken individually and is not rendered obvious by teachings of these two references when taken in combination. Claim 15, which is dependent upon claim 13, is allowable for the reasons discussed above with respect to claim 13, as well as on its own merit.

#### Conclusion

It is respectfully submitted that the claims as they have been amended are allowable over the art which has been applied in this Office Action. Favorable reconsideration and allowance of this application are courteously solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the

filng of this paper, including extension of time fees, to Deposit Account 07-1337 and  
please credit any excess fees to such deposit account.

Respectfully submitted,  
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